A root and branch

When it comes to designing a clock tree, what do you need to take into account? By Neil Tyler.

A clock tree is intended to generate the reference timing required by all the ICs in a PCB design and the challenge for an engineer is to design one with the fewest number of components possible, while at the same time meeting system-level performance requirements.

Design engineers need to take into account real estate restrictions – can they simplify complex PCB layouts? – and they have to be clear as to whether the clock generation IC is expected to do jitter attenuation or clock synthesis.

It is crucial then that the design starts with an understanding of the requirements of the application. What are the specific frequencies of interest? How many clocks will be required as result and what are respective signalling requirements of these clocks – single ended (LVCMOS) or differential (LVPECL, LVDS, CML, HCSL)?

According to James Wilson, marketing director of timing products for Silicon Laboratories: “Timing is traditionally a physical layer design challenge so, from a timing perspective, hardware designers should treat the other ICs in the system as a ‘black box’ and just focus on understanding the various IC timing requirements.”

In most consumer applications, system level functionality tends to be provided by highly integrated SoCs and these typically require only a low cost quartz crystal for reference timing. However, if the design has discrete peripheral components – say Ethernet or USB – then a single IC clock generator to provide reference timing for the SoC and the peripherals tends to be required.

“When it comes to designing for more complex embedded and communication applications designs tend to use a wide variety of ICs (processors, FPGAs, ASICs, PHYs, switches, DSPs and SoCs) and independent timing is needed for control plane processing and data path processing,” suggests Wilson.

“Some ICs can be driven by a single reference clock input, while some have multiple clock domains that need independent timing. These types of applications will require more complex clock trees, so engineers should be looking at a combination of oscillators, clock buffers and clock generators to complete their design.”

The type of clock tree that is required will depend on receiver requirements which will include: jitter performance, rise/fall time, duty cycle, signal amplitude and common mode voltage. Of these, jitter is the most important selection criterion.

**Strict jitter requirements**

“The design engineer will need to understand what the jitter requirement for each individual clock is,” explains Andreas Coucopoulos, senior product line marketing manager with Microsemi. “as strict jitter requirements will restrict what clock generators can be used in the clock tree – jitter of less than 300fs is required by many PHYs in the industry today.”

Wilson agrees. “Complex devices, such as high speed transceivers for Ethernet (10/40/100GbE) and Optical Transport Networking applications, as well as high speed data converters, require reference clocks with very low phase jitter and/or phase noise.”

According to Wilson, the system designer will first need to select reference timings for these jitter-critical clocks and suggests that implementations can range from using XO/VCXOs to high performance clock generators to drive these mission critical clocks.

“In synchronous systems, special jitter attenuating clocks are used to synchronise the local system to the rest of the network.”

The second most important selection criterion will be the frequency mix.

“If a single frequency is required, the most efficient solution is a simple XO or XO plus buffer,” he continued. “If a diverse mix of frequencies is required, a clock generator is often the most efficient solution. The
“Frequency flexible clock generators can replace quartz in most simple clock synthesis applications.”
Andreas Coucopoulos

Hardware designers should always compare clock generators’ fractional jitter performance against the application requirements and select the lower jitter option since it maximises design margin.

Simplifying the clock tree design is an important consideration. Engineers should not just be interested in highly efficient clock tree designs, but should also be looking to reduce the component count.

As a result, especially in consumer and computing applications, increasing numbers of engineers appear to be turning to cost effective single chip solutions that are capable of providing all clock synthesis and distribution.

Cutting the quartz elements
Issues of cost, reliability, performance and flexibility mean that design engineers are reducing the number of quartz elements in their systems. In response, traditional quartz companies have moved ‘upmarket’ into areas such as high specification TCXOs (temperature compensated crystal oscillators) and OCXOs (oven controlled crystal oscillators), which are being employed in wireless communications and mass data transfer applications.

“These types of devices offer sub ppm (parts per million) and ppb (parts per billion) stabilities, as well as very high noise performance in order to provide design integrity,” explains Peter Sinclair, engineering application support manager with IQD Frequency Products.

While there have been significant improvements in crystal design and manufacturing techniques, like mesa technology, which combines high performance with higher fundamental frequencies to allow design engineers to simplify circuits and improve effectiveness, are designers turning away from crystals and crystal oscillators?

Coucopoulos argues that they are. “Frequency flexible clock generators can replace quartz in most simple clock synthesis applications and tend to offer much greater design flexibility,” he says.

A case in point is IDT’s Versa Clock 5 family of programmable clock generators. This multi output low power timing solution has been designed to provide greater design flexibility. Its eight output programmable clock generator is capable of generating independent frequencies up to 350MHz in various output types and, with RMS phase jitter of less than 0.7ps over the full 12kHz to 20MHz integration range, it can meet the noise requirements of PCI Express Gen 1/2/3, USB 3.0 and 1G/10G Ethernet.

Wilson, however, believes that the use of silicon and quartz-based timing solutions are highly complementary.

“Low cost quartz crystals, for example, remain the most popular frequency source in consumer electronics because they offer excellent phase noise performance, small size and low cost,” explains Wilson. “Temperature compensated quartz solutions with excellent long term aging profiles, like TCXO and OCXO, are still being used to provide high stability references in wireless infrastructure and communication networks.”

One final consideration that design engineers should also bear in mind is that it is much easier to source one device – lead times for crystals are increasing as production processes become more complicated – than multiple crystals when designing for multiple frequencies in more complex applications.