Continuous change

Despite an apparent false start a decade ago, programmable analogue is making a resurgence – and memristors could be the driver. By **Chris Edwards**.

Some of the earliest computers used for controlling processes featured analogue architectures because they were much more responsive than valve based logic circuits. But they needed to be custom designed and succumbed to the more flexible – and ultimately cheaper – digital computer.

However, advances in programmable analogue technology may see not just the resurgence of analogue computing in areas where digital works out to be more power hungry, but also a way of supporting analogue functions on increasingly dense but highly variable SoCs.

There are two grades of programmable analogue. One has already become a part of mainstream chip design. This is digitally assisted analogue, where on chip calibration and adjustment circuits can tweak the behaviour of the analogue section and reduce the effects of noise and component mismatches.

The idea behind digital assistance is to replace precision circuitry that makes extensive use of analogue feedback with simpler alternatives and backs them up with digital control to linearise the signal. For example, researchers at UC Berkeley proposed about a decade ago to liberate the high gain amplifier lurking inside a conventional op amp, which through the use of feedback has a gain orders of magnitude lower. Using an open loop digital calibration technique, despite the massive intrinsic non linearity of the design, digital control succeeded in producing a usable output with significant power savings on deep sub micron processes. In terms of power as well as area, scaling tends to favour a shift towards digital, particularly for low frequency designs.

One issue the researchers noticed was that analogue circuitry became far more temperature dependent, with local, signal driven heating contributing significantly to inaccuracies. So layout needed to take into account how transistors would heat up under load. The solution was to intersperse components with different heat profiles to avoid hot spots. More recent research at Chalmers University into wideband RF amplifiers built on gallium nitride has shown that DSPs that take the temperature models into account can accommodate thermally driven changes in analogue behaviour.

The other form of programmable analogue remains more experimental, with circuitry realised on field programmable analogue arrays (FPAAs). This has seen less success commercially so far, although there have been some niche successes. A number of products that made it to market a decade or more ago have been withdrawn or put on the end of life list. For example, the ispPAC devices developed by Lattice Semiconductor were hit by a recent fab closure and the TRAC020 from Zetex – now part of Diodes – failed to
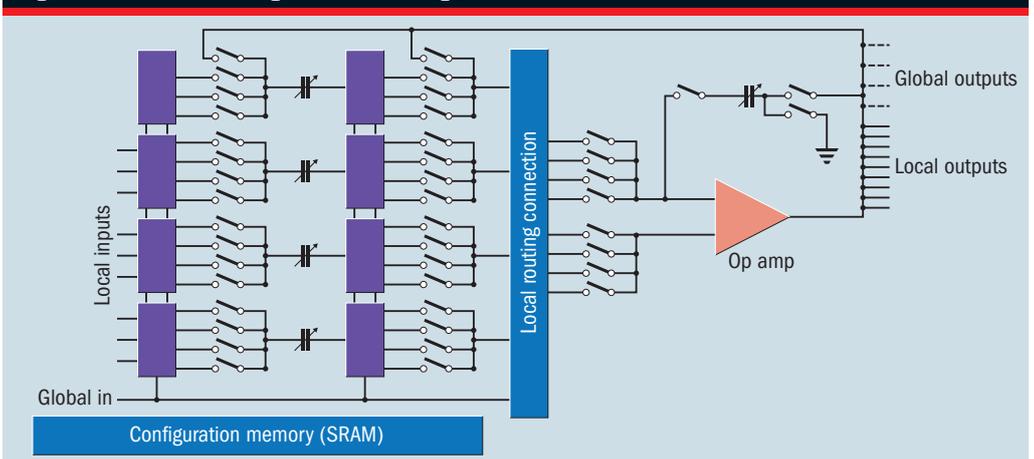
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make it past the shift to lead free construction. Although its FPAAs are 'end of life', Anadigm has carried over the programmable analogue approach originally developed by Pilkington in the 1990s to the dsASP family, which can be reconfigured dynamically under the control of an external microprocessor or digital controller to allow live manipulation of the circuitry.

Research, however, continues into uncommitted analogue arrays as changes to process technology and the arrival of new fundamental devices, such as the memristor, make the concept more feasible. Other researchers have developed methods for analogue computing and control that are potentially faster and less power hungry than digital counterparts – using the convergence of voltages and currents in a network to solve simultaneous equations or to perform optimisations.

Analogue arrays split into two groups: continuous time; and discrete time. Anadigm remains the key commercial architecture for discrete time programmable analogue, using a network of switched capacitor sub

Fig 1: The basic configurable analogue block

Local inputs · Global in · Configuration memory (SRAM) · Local routing connection · Op amp · Global outputs · Local outputs

circuits, similar to those found in A/D converters fabricated on CMOS processes (see fig 1). The switches are easy to control digitally and allow effective resistances and capacitances to be tuned without having to alter their physical dimensions. Switched capacitor blocks are arranged around conventional op amp circuits, providing the programming needed to implement typical feedback controlled analogue circuits.

Continuous time

Although switched capacitor circuitry is a good match for CMOS, switching imposes a limit on the achievable bandwidth of the circuit. Continuous time architectures can, in principle, process higher frequency signals. Zetex' TRAC architecture achieved bandwidths more than an order of magnitude higher than its switched capacitor peers in the late 1990s and early 2000s. One architecture developed at the University of Freiburg in the last five years, has achieved unity gain of close to 200MHz.

The continuous time approach hit a setback from the loss of the Lattice and Zetex parts, but research continues, generally revolving around the use of transconductance amplifiers. In recent years, researchers have either favoured continuous time architectures or opted for a hybrid approach that incorporates a wider range of analogue building blocks.

The RASP, developed at Georgia Institute of Technology, is based on a smorgasbord of integrated components that include folded Gilbert cell multipliers and programmable offset transconductors, as well as simple NMOS and PMOS transistors (see fig 2). The programming elements are floating gate transistors which, although normally used digitally or to represent a small set of values, can be used as configurable analogue components. Because the floating gate transistors are embedded in a large routing array, the parasitics of the crossbar network can affect the circuit parameters so the team implemented routing lines of different lengths to allow a reasonable resistance and capacitance to be selected as the control for each active analogue subcircuit. So far, however, designs such as this have not crossed into the commercial world, where the focus is on much more limited control over analogue subcircuits.

The recognition that most analogue circuitry now drives a digital core has led to the appearance of devices such as Cypress Semiconductor's PSoC and, more recently, Maxim Integrated's MAX11300. These put a series of analogue building blocks onto a digital chip. In the case of the PSoC, analogue functions are under the control of an on chip microcontroller. The Maxim part, meanwhile, is configured at design time to link different mixed signal elements such as A/D and D/A converters together directly.

Memristors are now driving the development of potentially much denser analogue neuromorphic computers

A driver for FPAAs may come from new forms of computing. One of the early applications for the devices was in neural network research and resurgent interest in brain science, driven by programmes such the Human Brain Project, is seeing the development of neuromorphic, self programming architectures that use analogue, rather than digital, processing. Researchers at the University of Heidelburg are building a wafer scale model of the brain using an interconnect structure similar to that of an FPGA. Like the RASP, the neurons store their 'learned' data on a floating gate element.

Following their successful creation at HP Labs, memristors are now driving the development of potentially much denser analogue neuromorphic computers. Professor Leon Chua of the University of California, who predicted the existence of memristor behaviour in nature – a state dependent change in the resistance of a device to electricity – claimed at the 2012 DATE Conference that much of the behaviour of the Hodgkin-Huxley model of the neuron, which has been used by neuroscientists for decades, could be emulated by a memristor.

By combining attributes of spintronic transistors and memristors, a team from the Polytechnic of New York University has shown that arrays could perform shape and character recognition with 100 times better energy efficiency than digital implementations.

Because they can be formed into crossbar architectures easily, memristors could form the basis of highly dense neurocomputers and even more general purpose analogue arrays, particularly those that need some way to store data locally in analogue form.

However, there is one key problem: manufactured devices suffer from high variability. Before they can become viable commercially, production processes have to improve dramatically, although digital calibration and linearisation might help. If they succeed, the memristor could underpin new classes of programmable analogue designs.

Fig 2: Examples of the CABs developed by the RASP team