Succesive approximation A/D converters, with resolutions of up to 18bit and sampling at 10Msamples/s, are suited to many data acquisition applications. They have four main elements: the sample and hold amplifier (SHA); an analogue comparator; a reference D/A converter; and the SAR (successive approximation register). Because the SAR controls the operation, they are often called SAR converters (see fig 1).

After power up and initialisation, a signal starts the conversion cycle. The switch closes, connecting the analogue input to the SHA, which acquires the input voltage. When the switch opens, the comparator determines whether the analogue input – now stored on the hold capacitor – is greater or less than the D/A converter voltage.

At first, the most significant bit (MSB) is on, setting the D/A converter’s output voltage to midscale. After the comparator output has settled, the SAR turns off the SHA if the D/A converter’s output is larger than the analogue input, or keeps it on if it is smaller. The process repeats with the next MSB and this binary search continues until every bit in the register is tested. The resulting D/A converter input is a digital approximation of the sampled input voltage and is output by the A/D converter at the end of the conversion.

Some A/D converters that operate with multiple supplies have well defined power up sequences and AN-932 provides a good reference for designing power supplies for these converters. Special attention should be paid to the analogue and reference inputs; typically, these should not exceed the analogue supply voltage by more than 0.3V. Thus,

\[ AGND – 0.3V < V_{in} < V_{DD} + 0.3V \]

\[ AGND – 0.3V < V_{ref} < V_{DD} + 0.3V \]

Analogue supplies should be turned on before the analogue input or reference voltage, otherwise the analogue core could power up in a latched up state. Similarly, the digital inputs should be between DGND – 0.3V and \( V_{IO} + 0.3V \). The I/O supply must be turned on before (or at the same time as) the interface circuitry or ESD diodes on these pins could become forward biased and power up the digital core in an unknown state. Do not access the A/D converter before the power supplies are stable, as this may put it into an unknown state.

Many SAR A/D converters, such as the AD760x and the AD765x-1, require a RESET for initialisation after power up. Once all power supplies are stable, a specified RESET pulse should be applied to guarantee the A/D converter starts in the intended state, with digital logic control in the default state and the conversion data register cleared. Upon power up, voltage builds on the REF\(_{in}/\text{REF}_{out}\) pin, the A/D converter is put into acquisition mode and the user specified mode is configured. Once fully powered, the AD760x should see a rising edge RESET pulse – typically 50ns wide – to configure it for normal operation.

The A/D converter converts the analogue input voltage to a digital code – the reference voltage – which must be stable before the first conversion. A poorly designed reference circuit can cause serious conversion errors. The most common reference problem is ‘stuck’ codes, which may be caused by the size and placement of the reservoir capacitor, insufficient drive strength or a large amount of noise on the input.

For multichannel, multiplexed applications, the driver amplifier and the A/D converter’s analogue input circuitry must settle to the 16bit level (0.00076%) for a full scale step on the internal capacitor array. Unfortunately, amplifier datasheets typically specify settling to 0.1% or 0.01%. This could differ significantly from the settling time at a 16bit level, so verification is required prior to driver selection.

Pay special attention to settling time in multiplexed applications; after the multiplexer switches, make sure there is enough time for the analogue input to settle to the specified

**Analogue supplies should be turned on before the analogue input or reference voltage, otherwise the analogue core could power up in a latched up state.**

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**Fig 1: A basic SAR A/D converter architecture**

- **Timing**
  - **Reset**
  - **Convert**
  - **EOC, DRDY or busy**

- **Control logic: successive approximation register**
  - **Output** parallel/serial

- **D/A converter**

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**Sample and hold amp**

- **Analogue input**

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25 March 2014 www.newelectronics.co.uk
accuracy before the conversion starts.

When using the AD7606 with a multiplexer, allow at least 80µs for the ±10V input range and 88µs for the ±5V range to give the selected channel enough time to settle to 16bit resolution.

Make sure the analogue input is within the specified input range, taking special care of differential input ranges with a specified common-mode voltage. For example, the differential input range of the AD7960, an 18bit, 5Msample/s SAR A/D converter, is –VRF to +VRF, but both VIn+ and VIn– referred to ground should be in the range from –0.1V to VRF + 0.1V and the common mode voltage should be around VRF/2.

To conserve power, some SAR A/D converters go into power down or standby mode when idle, so make sure the converter comes out of this mode before the first conversion starts.

For example, the AD7606 family offers two power saving modes: full shutdown and standby. These modes are controlled by GPIO pins STBY and RANGE. When STBY and RANGE return high, the AD7606 goes from full shutdown mode into normal mode and is configured for ±10V range (see fig 2). At this point, the REGCAPA, REGCAPB, and REGCAP pins power up to the voltages outlined in the datasheet. When placed in standby mode, power up takes approximately 100µs, but it takes approximately 13ms in external reference mode. When powered up from shutdown mode, a RESET signal must be applied after the required power up time has elapsed. The datasheet specifies the time required between power up and a rising edge on RESET as ‘wake-up shutdown’.

While it is commonly believed that SAR A/D converters have no latency delay, some have such a delay for configuration updates, so the first valid conversion code may be undefined until the delay – which may be several conversion periods – has passed.

The AD7985 features two conversion modes: turbo and normal. Turbo mode, which allows conversion rates of up to 2.5Msamples/s, does not power down between conversions, so the first conversion contains meaningless data and should be ignored. In normal mode, however, the first conversion is meaningful.

For the AD7682/AD7689, the first three conversion results after power up are undefined, as valid configuration does not take place until after the second EOC. Therefore, two dummy conversions are required (see fig 3).

When using the AD765x-1 in hardware mode, the logic state of the RANGE pin is sampled on the falling edge of the BUSY signal to determine the range for the next simultaneous conversion. After a valid RESET pulse, the AD765x-1 defaults to operating in the ±4 × VRF range, with no latency problem. If, however, in the ±2 × VRF range, one dummy conversion cycle must be used to select the range at the first falling edge of BUSY.

Some oversampled SAR A/D converters have postdigital filters that cause additional latency delay. When multiplexing analogue inputs to this type of converter, the host must wait for the full digital filter settling time before a valid conversion result can be achieved; after this, the channel can be switched.

Last, but not least, the host can access the conversion results through some common interface. To get valid conversion data, make sure the digital interfacing timing specifications in the datasheet are followed.

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