SuperChip initiative meets SoC design needs.

By Grant Martin and Henry Chang.

"The increased complexity of AMS-SoC designs means they are thought of as today's 'SuperChips'."

R  estimated demand for smaller, cheaper and lower power consumer products drives designers to combine the fundamental analogues, RF and mixed signal components of communications products into a single chip on a SoC. The design of future SoCs necessitates a fusion of what were separate disciplines. Those who used to work separately must now collaborate in critical areas of the design.

The design flow demands more than just a comprehensive collection of point tools for system design, IC design, PCB design and embedded software development. It requires a tightly integrated array of complex, cross-disciplinary design solutions that are cooperation among large and diverse design teams.

The move to SoC design

Figure 1 shows a typical consumer product, comprising numerous micros (the hardware) and the embedded software that runs on this hardware. The embedded software layer consists of several components, including the application software or threads, an application program interface (API), hardware drivers and a kernel that provide the underlying infrastructure for all of these components. There is a critical gap between the software and the hardware, with a large gap in software development between the hardware and the embedded software that runs on the hardware. The hardware typically includes the PCB and packaging ICs, which incorporate the various components shown in Figure 1. The constituent parts of the ICs are managed by glue logic (or in software tools, the scheduler). These components are usually combined into one or more ICs, depending on cost and time to market constraints. Market requirements drive the exact configuration and content for the end products. Time to market, cost and process technology capabilities determine the level of integration in the end products. Many of today's communication products require high levels of integration, which forces designers to integrate many hardware components onto a single SoC.

SuperChip mixed signal design

There are two fundamental SoCs. The first, which grows from the ASIC world, is mostly digital and may contain some analogue/mixed signal blocks, or IP. Treated as black boxes, these chips are owned by the digital designer and are called 'big D-little a' or ASIC SoCs. These have grown to a point where the cost of 100% handcrafting is prohibitive. These larger designs also require synthesis and routen the analogues, and the incorporation of microprocessor and digital core chips. This type of SoC, dominated by digital designers, is driven by the custom or a computer and designer and called a 'big A-little d' or AMS-SoC. The increased complexity of AMS-SoC design requires a more thoughtful approach to and physical realisation of analogue designs with these tools is largely a manual process.

On the digital side, current tools do not take sufficient account of physical effects during the layout and planning design phases. This results in designs that cannot meet their constraints when implemented and so require costly design rework. Whilst these specific limitations are being addressed at a localised level, the lack of interaction between the digital and analogue design processes is more significant. Digital and analogue design tools tend to be tailored only to their specific design methodologies and frequency do not take into account the effects of coupling with their counterparts.

System level AMS-SoC design

Definition of system functionality is the emphasis in system level design. The process supports a number of key stages in the initial design: • definition and modelling of an appropriate architecture onto which the functional model will be mapped; • assessment of the suitability of this architecture and implementation platform.

This concept was developed for software and digital hardware co-design. But, to support SuperChip AMS-SoC design, it must extend to encompass generalised system tradeoffs and analysis between additional domains of processing: RF, analogue and digital hardware.

The design of future SoCs necessitates a multi-year cooperative effort with leading SoC design organisations. The goal is to provide them with the most advanced design tools and infrastructure that takes into account the complexities of the design and the latest techniques to support the design.

Sponsored Tutorial

A multi-year cooperative effort with leading SoC design organisations. The goal is to provide them with the most advanced design tools and infrastructure that takes into account the complexities of the design and the latest techniques to support the design.

Figure 1: Breakdown of a typical consumer product

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Breakdown of a typical consumer product

Software

Hardware

External Interface

Control

Drivers

API

Boot Sequencer

Glue Logic/Scheduler

I/O

RF

BIOS

Buses

Data

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The Cadence SuperChip initiative is a multi-year cooperative effort with leading SoC design organisations. The goal is to provide them with the most advanced design tools and infrastructure that takes into account the complexities of the design and the latest techniques to support the design.