Providing a window into SoCs

Rupert Baines tells **Neil Tyler** about a transformation in the way in which next generation devices and systems are delivered.

Those in the telecoms sector may know of Rupert Baines from his time as chief marketing officer of picoChip which, before it was acquired by Mindspeed, was developing products for 4G and developing the concept of small cell communications.

With more than 25 years' experience working in technology marketing and in commercialising technologies, Baines has worked in a variety of businesses – from start ups to blue chips – as welll as with venture capitalist Pond Ventures. At Analog Devices, he played a key role in the development and mass market adoption of digital subscriber line (DSL) – the broadband access technology.

Last year, he was appointed CEO of UltraSoC, a Cambridge based company specialising in the development of debugging and analytic technology for embedded systems.

Investors in the business include Octopus Investments, which has helped companies like Zoopla Property Group, Secret Escapes and Swiftkey to build globally successful businesses.

According to Baines: "UltraSoC is looking to transform the way in which companies develop and deliver next generation devices and systems.

"It specialises in semiconductor IP that is licensed into big complicated digital chips. Modern chip designs are insanely complicated, with dozens of cores, hundreds of different IP blocks, billions of transistors and multiple vendors. Whether it's multiprocessing units, GPUs, DSPs, or third party IP blocks, there's been a massive increase in complexity. Knowing what is going on inside your SoC is fiendishly difficult – it is just really hard."

As a result, it is often impossible to predict the behaviour of an SoC. "What UltraSoC can do is to enable development teams to look inside SoCs during the development process so they can not only see, but also understand, how the device operates in a real world situation.

"Most people today use a combination of JTAG – which, while it may be universal, is quite primitive and slow – and an in house architecture. What UltraSoC provides is a modern architecture that has been designed explicitly for complex devices. It lets you touch all the different elements in the SoC – cores, coprocessors and graphic units – and then brings out the necessary information in a rich and useful way."

The IP has been designed to go onto the die at the design stage in the form of blocks which help to debug the device, as well as get the hardware working and the hardware and software working together.

Spun out of Essex and Kent universities UltraSoC was set up ten years ago. "The company was set up to create a development methodology that puts some intelligence into the chip so that you are better placed to understand what is going on. It is a really clever bit of IP which, in many respects, was ahead of its time," suggests Baines.

In terms of IP support, the company has a library of some 30 components. "That means we can touch almost anything in a standard device. We can support ARM, MIPS, CEVA and Tensilica cores, amongst others. We can support different bus protocols – just about anything really. We also work across different power and clock domains, with the aim of supporting the complex design environment in which designers operate today."

Baines sees the company's IP as 'game changing'. "It will help designers to refine the operation of their products when they are in use and that's not really been possible before.

"By embedding debug and analysis capabilities in silicon, designers will be able to debug their devices more quickly and integrate new features, for example, service power optimisation and failure detection.

"UltraSoC has had a good reaction from customers. For a typical 18 month project, we have been able to cut development time by two months and, when you consider the fact that a third of a project's time can be spent on debugging, that is significant. It means a project could be saving hundreds of thousands of pounds in development costs and getting its product to market significantly earlier than the competition."

Since his appointment in April 2015, Baines has been focusing on raising the profile of the company and its technology.

"If I'm honest, the previous management team came with an engineering approach. The messaging was focused on how good the technology was, rather than it had developed a solution to address a problem and delivering what was needed. That's not a problem unique to UltraSoC; from the jet engine onwards, it's been a problem that many UK technology businesses have had to address.

"The technology is great, the engineering team is good. What the company needed was someone who understood the market and could translate a great technology and take it to the next level."

In January 2016, the company appointed four technology business leaders to its strategic advisory board – between them, Simon Davidman, Guillaume d'Eyssautier, Vijay Dube and Professor David May have helped to establish and exit a dozen start ups and have worked with a host of high profile companies.

At the time, Baines said they would bring a visionary approach to big problems, as well as technological excellence and entrepreneurial skill.

"We have developed a 'smart' vendor neutral approach that will help developers to control and monitor any on chip structure in active operation. These are the capabilities that are essential in modern design," concludes Baines.

"We are now well placed to help designers deliver products more quickly, while ensuring their device and its software are functioning correctly."

Rupert Baines

Rupert Baines has worked in the semiconductor and communications industries for more than 30 years and has held senior roles in start ups and prominent trans-national companies.
Before joining UltraSoC, he was VP of strategic marketing at Mindspeed, following that company's acquisition of Picochip (now part of Intel), where he had served as VP of marketing. His CV includes spells at first:telecom, Arthur D Little and Analog Devices.